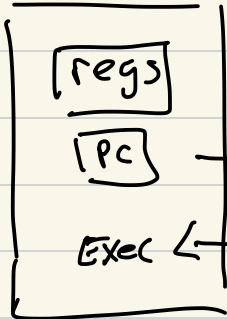
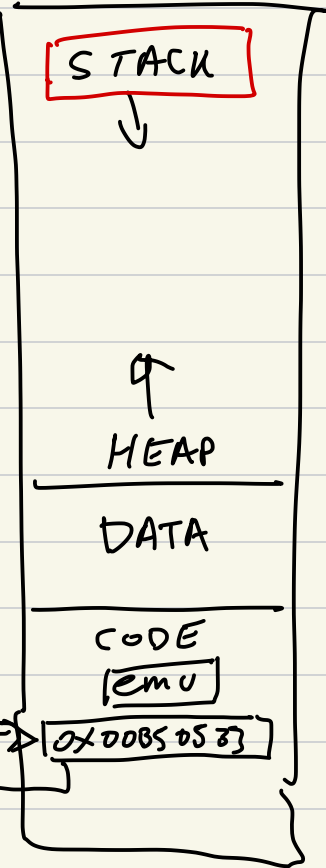


# CS 631-02 RISC-V Emulation

RISC-V  
Processor



Memory

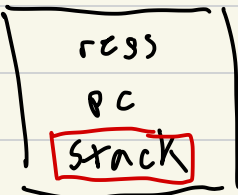


add a0,a0,a1

RISC-V

Emulation  
(code)

struct state



emu

processor  
state

code

# RISC-V Emulator Implementation

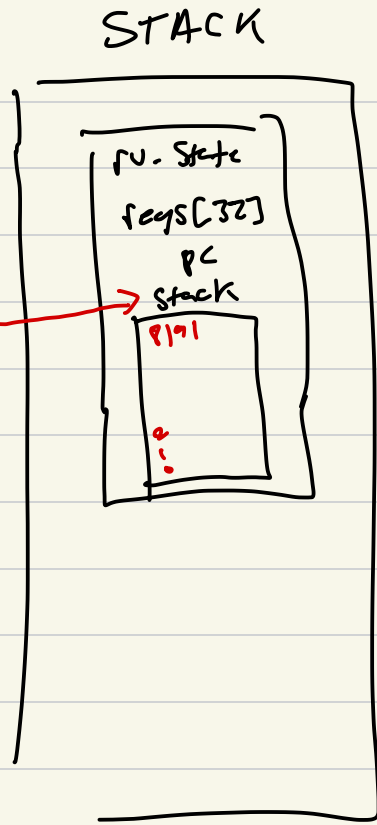
## Incremental Development

- ① Identify an instruction : ADDI
- ② Identify the instruction format  
i-type
- ③ Implement or add to current implementation
- ④ Decode Iw  
get fields
- ⑤ Construct immediate  
from Iw
- ⑥ Update state  
update rd  
update memory  
update PC

init Stack

emulated

SP



new instruction formats

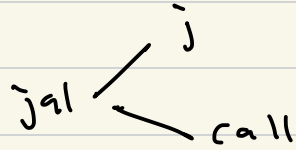
immediates

jumps and branches

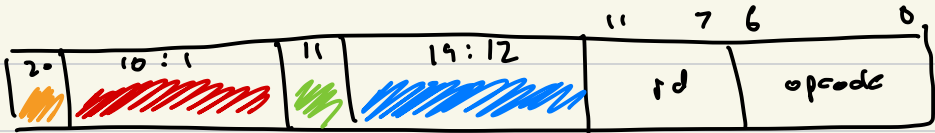
memory

# JAL

J-type immediate



## IW



## imm21



$$\text{int64}_t \text{ imm64} = \text{sign-ext}(\text{imm21}, \underline{20})$$

## B-type

beq rs1, rs2, label

LW lw rd, offset(rs1)

$$\text{uint64}_t \text{ target\_addr} = \underline{\text{base}} + \text{offset}$$

$$\text{uint64}_t \text{ value} = *((\text{uint32}_t *) \text{target\_addr});$$